WE CLAIM

1. A method for optimization of apodization circuits comprising:

providing an apodization circuit;

replacing a multiplier within the apodization circuit with a first replacement multiplier; and

replacing a window function of the apodization circuit with a first replacement window function.

2. The method of claim 1 wherein the providing of the apodization circuit comprises selecting the apodization circuit from a plurality of apodization circuits.

3. The method of claim 1 further comprising selecting the first replacement multiplier from a plurality of replacement multipliers.

4. The method of claim 1 further comprising the replacement of the multiplier by a memory device where all possible outcomes of the first replacement multiplier are stored.

5. The method of claim 1 wherein the first replacement window function is compatible with the first replacement multiplier.

6. The method of claim 1 further comprising:

applying a noise shaping technique to the window function of the selected apodization circuit; and

creating a first replacement window function based on the noise shaping technique of the window function of the apodization circuit.

7. The method of claim 1 further comprising:

applying the apodization circuit to a provided plurality of transducers;

applying an electric pulse to the plurality of transducers wherein the electric pulse is applied to each transducer within the plurality;

measuring the responses of the plurality of transducers based on the electric pulse applied to each transducer; and

applying a noise shaping technique to the window function of the selected apodization circuit, wherein the noise shaping technique accounts for the responses of the transducers.

8. The method of claim 1 further comprising determining a first efficiency rate for the apodization circuit with the first replacement multiplier and the first replacement window function.

9. The method of claim 8 further comprising:

replacing the first replacement multiplier within the apodization circuit with a second replacement multiplier;

replacing the first replacement window function within the apodization circuit with a second replacement window function;

determining a second efficiency rate for the apodization circuit with the second replacement multiplier and the second replacement window function;

comparing the first efficiency rate with the second efficiency rate; and

selecting between the apodization circuit with the first replacement multiplier and the first replacement window function and the apodization circuit with the second replacement multiplier and the second replacement window function, based on the comparing of the first efficiency rate with the second efficiency rate.

10. The method of claim 9 wherein the second replacement window function is suitable for use with the second replacement multiplier.

11. A system for optimization of apodization circuits comprising:

means for providing an apodization circuit;

means for replacing a multiplier within the apodization circuit with a first replacement multiplier; and

means for replacing a window function of the apodization circuit with a first replacement window function.

12. The system of claim 11 wherein the apodization circuit is selected from a plurality of apodization circuits.

13. The system of claim 11 further comprising means for selecting the first replacement multiplier from a plurality of replacement multipliers.

14. The system of claim 11 further comprising:

means for applying a noise shaping technique to a window function of the apodization circuit; and

means for creating a first replacement window function based on the noise shaping technique of the window function of the selected apodization circuit.

15. The system of claim 11 further comprising means for determining a first efficiency rate for the selected apodization circuit with the first replacement multiplier and the first replacement window function.

16. The system of claim 15 further comprising:

means for replacing the first replacement multiplier within the apodization circuit with a second replacement multiplier;

means for replacing the first replacement window function within the apodization circuit with a second replacement window function;

means for determining a second efficiency rate for the apodization circuit with the second replacement multiplier and the second replacement window function;

means for comparing the first efficiency rate with the second efficiency rate; and

means for selecting between the apodization circuit with the first replacement multiplier and the first replacement window function and the apodization circuit with the second replacement multiplier and the second replacement window function, based on the comparing of the first efficiency rate with the second efficiency rate.

17. A computer-usable medium storing a computer program, comprising:

computer-readable program code for providing an apodization circuit;

computer-readable program code for replacing a multiplier within the apodization circuit with a first replacement multiplier; and

computer-readable program code for replacing a window function of the apodization circuit with a first replacement window function.

18. The computer-usable medium of claim 17 wherein the apodization circuit is selected from a plurality of apodization circuits.

19. The computer-usable medium of claim 17 further comprising computer-readable program code for selecting the first replacement multiplier from a plurality of replacement multipliers.

20. The computer-usable medium of claim 17 further comprising:

computer-readable program code for applying a noise shaping technique to a window function of the apodization circuit; and

computer-readable program code for creating a first replacement window function based on the noise shaping technique of the window function of the apodization circuit.

21. The computer-usable medium of claim 17 further comprising computer-readable program code for determining a first efficiency rate for the apodization circuit with the first replacement multiplier and the first replacement window function.

22. The computer-usable medium of claim 21 further comprising:

computer-readable program code for replacing the first replacement multiplier within the apodization circuit with a second replacement multiplier;

computer-readable program code for replacing the first replacement window function within the apodization circuit with a second replacement window function;

computer-readable program code for determining a second efficiency rate for the apodization circuit with the second replacement multiplier and the second replacement window function;

computer-readable program code for comparing the first efficiency rate with the second efficiency rate; and

computer-readable program code for selecting between the apodization circuit with the first replacement multiplier and the first replacement window function and the apodization circuit with the second replacement multiplier and the second replacement window function, based on the comparing of the first efficiency rate with the second efficiency rate.